Searched the web for **["bus transactions" and "test cases"]**. Results **21 - 30** of about **104**. Search took **0.15** se

[PDF] XAPP246 "PowerPC 60X Bus Interface to a Virtex-E Device" v1.0 (...
File Format: PDF/Adobe Acrobat - View as HTML
... Pipeline The address pipeline permits overlapping address **bus transactions** on the ... environment,
the designer is extremely productive at generating **test cases**. ...
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... transfer of data rather than adding additional latency in the PCI **bus transactions**. ... in the SPACE 2 platform and measured its performance in **test cases** and when ...
www.cis.unisa.edu.au/~cisdak/ResearchPapers/ ACACHigh1999.ps - Similar pages

[PS] Coverage-Directed Test Generation UsingSymbolic Techniques Daniel ...
File Format: Adobe PostScript - View as Text
... language code. Simulation environments for ASICs may have **test cases** written in terms of **bus transactions**. The translation process ...
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[PDF] Verification, Characterization, and Debugging of the HP PA 7200 ...
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... years running at operational speed to hit all the interesting **test cases**. ... to do exhaustive testing of the effects of various **bus transactions** interacting with ...
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... the number of clock cycles used to per- form various **bus transactions** and can ... part (test_sw) of this example consists of several **test- cases** to interactively ...
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... of the number of clock cycles used to perform various **bus transactions** and can ... part (test_sw) of this example consists of several **test-cases** to interactively ...
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... **Transactions** 33Mhz @ 32 bits Utopia I @ 32 bits @ 8 bits Device Under Test (DUT) 125Mhz Micron Models 25Mhz ATM Packet Generator System Testbench **test cases** ...
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[PDF] Intel GW80314 I/O Processor DMA and XOR Library
File Format: PDF/Adobe Acrobat - View as HTML
... The testbench provides menu driven **test cases** implementing the Libraries. ... The **bus**

transactions created by the DMA/XOR block are handled by the controllers. ...
www.intel.com/design/iio/papers/25367501.pdf - Similar pages

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... such as read() or write() and translates them into **bus transactions** that model ... must be given to guard against duplicate, irrelevant, and illegal **test cases**. ...
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... Its role is to make sure that the **bus transactions** issued by upper V_Layers will reach the DUT, regardless of how the DUT is represented. ...
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[PDF] Coverage-Oriented Verification of Banias
File Format: PDF/Adobe Acrobat - View as HTML
... random testing, without embellishing corner cases or careful crafting delicate **test cases**. ... we required the coverage of back-to-back **bus transactions** that were ...
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... protocols are used to specify the exact manner in which **bus transactions** occur. ... profiles for the MAC processor for a large number of **test cases**, consisting of ...
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[PDF] Functional Verification of the HP PA 8000 Processor
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... 1 Each job ran several thousand **test cases** that were generated using a ... emulate the functionality required to initiate and respond to **bus transactions**, but the ...
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[PDF] 1394.1 Standards Meeting Minutes
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... you must wait for a (broadcast) notification before you resume off-**bus transactions**. ... 1.11.4 Presenter: David V. James, Sony ∑ Slides of **test cases** needed to ...
grouper.ieee.org/groups/1394/1/Minutes/jul99.pdf - Similar pages

[PDF] Debug Methodology for the McKinley Processor
File Format: PDF/Adobe Acrobat - View as HTML
... Small **test cases** of 100's of instructions are run on the processor ... that it would fail to properly operate during initial **bus transactions** immediately after ...
www.intel.com/design/itanium2/download/debug_paper.pdf - Similar pages
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<html> <head> </head><body><pre><html> <head> </ ...
... since it is either returning data or forwarding XMI2 **bus transactions** for potential ... in catching two design flaws that the focused **test cases** had missed. ...
research.compaq.com/wrl/DECarchives/ DTJ/DTJ704/DTJ704SC.TXT - 45k - Cached - Similar pages

[PDF] TeX output 1995.03.21:1529
File Format: PDF/Adobe Acrobat - View as HTML
... A bus demon might generate random (but legitimate) **bus transactions** while the connected CPU ... they bias the random selection of system- level **test cases** in the ...
www-inst.eecs.berkeley.edu/~cs152/ handouts/clark-test.pdf - Similar pages

Verification Guild Archive, Vol 2, no 9
... the automatic generation of assembly language instructions or streaming together

bus transactions. ... and you have the ability to have **test cases** steer themselves ...
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... **Bus transactions** By keeping track of the number of **bus transactions** we hoped ... very deterministic pattern of sharing, which make them ideal **test cases** for Thor's ...
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Functional verification of the POWER4 microprocessor and POWER4 ...
... created several years ago to help us gauge the effectiveness of our **test cases**. ... It can analyze and report on a series of **bus transactions**, looking for specific ...
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- **149** articles found for: *"bus transactions"*

All sources | Scholarly Journals | Trade Publications | Newspapers

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1. **Serial-bus debugging in a parallel universe**
   Dan Strassberg, Pete Shumway, Anil Godbole. **EDN.** Boston: Oct 30, 2003. Vol. 48, Iss. 24; p. 51
   Text+Graphics | Page Image - PDF | Citation

2. **Revolution comes to SoC methods**
   Tim Herbert. **Electronic Engineering Times.** Manhasset: Sep 29, 2003. p. 50
   Text+Graphics | Page Image - PDF | Abstract

3. **Co-emulation rides standard to new heights**
   David Maliniak. **Electronic Design.** Cleveland: Sep 15, 2003. Vol. 51, Iss. 20; p. 46
   Text+Graphics | Page Image - PDF | Abstract

4. **Crossing the abyss: Asynchronous signals in a synchronous world**
   Mike Stein. **EDN.** Boston: Jul 24, 2003. Vol. 48, Iss. 16; p. 59
   Text+Graphics | Page Image - PDF | Abstract

5. **Show time for ESL design?**
   Richard Goering. **Electronic Engineering Times.** Manhasset: Jun 30, 2003. p. 18
   Text+Graphics | Page Image - PDF | Abstract

6. **CoWare to unveil native SystemC tool**
   Richard Goering. **Electronic Engineering Times.** Manhasset: May 5, 2003. p. 45 (2 pages)
   Text+Graphics | Page Image - PDF | Abstract

7. **Emulator's co-verification features get a boost**
   Michael Santarini. **Electronic Engineering Times.** Manhasset: Mar 3, 2003. p. 43 (1 page)
   Full text | Page Image - PDF | Abstract

8. **RISCy business**
   Jim Turley. **Embedded Systems Programming.** San Francisco: Mar 2003. Vol. 16, Iss. 3; p. 37 (3 pages)
   Text+Graphics | Page Image - PDF | Abstract

9. **Verification and debug instruments move on-chip**
   Electronic Engineering Design. Tonbridge: Nov 30, 2002. p. 49
   Full text | Abstract

☐ 10. **Interconnect IP steers SoC integration into the fast lane**
David Maliniak. **Electronic Design.** Cleveland: Nov 25, 2002. Vol. 50, Iss. 25; p. 45 (3 pages)

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11. **Interfacing VHDL and Verilog designs to C++ models**
Donna Mitchell. **ECN.** Radnor: Nov 15, 2002. Vol. 46, Iss. 13; p. 89 (1 page)
Text+Graphics | Page Image - PDF | Abstract

12. **Serial ATA**
Rob Calvin. **Computer Technology Review.** Los Angeles: Nov 2002. Vol. 22, Iss. 11; p. 14 (3 pages)
Text+Graphics | Page Image - PDF | Abstract

13. **TRADE NEWS: Agilent Technologies' New High-Speed Logic Analyzer Modules and Probes Provide Industry-Leading Insight for Emerging Technologies**
Business Editors/High-Tech Writers Intel Developer Forum 2002. **Business Wire.** New York: Sep 9, 2002. p. 1
Full text | Abstract

14. **Co-verification speeds SOC design**
Jason Andrews. **EDN.** Boston: Sep 5, 2002. Vol. 47, Iss. 19; p. 95 (4 pages)
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15. **Xilinx Debuts Industry's First IBM CoreConnect Integrated Bus Analyzer For Real-Time, On-Chip Debug and Verification**
PR Newswire. New York: Aug 26, 2002. p. 1
Full text | Abstract

16. **Method ensures on-track designs**
Michael Howard, Harry Foster, John Emmitt. **Electronic Engineering Times.** Manhasset: Aug 19, 2002. p. 55 (4 pages)
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17. **Mai Logic Incorporated Introduces Revolutionary Bus-Centric PowerPC System Controllers**
PR Newswire. New York: Jul 18, 2002. p. 1
Full text | Abstract

18. **Stacking up the JOLs**
Dominic Jones. **Asset Finance International.** London: Jun 2002. p. 12
Full text | Abstract

19. **Get on the bus**

☐ *Richard Ball.* **Electronic News.** New York: May 27, 2002. Vol. 48, Iss. 22; p. 18 (2 pages)

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☐ 20. **Altera Ahead of the Pack with Excalibur Solutions**
PR Newswire. New York: May 6, 2002. p. 1

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21. **USB debut tips**
Jan Axelson. **Embedded Systems Programming.** San Francisco: Apr 2002. Vol. 15, Iss. 4; p. 36 (5 pages)
Text+Graphics | Page Image - PDF | Abstract

22. **VSIA takes hard look at embedded software reuse**
Richard Goering. **Electronic Engineering Times.** Manhasset: Mar 4, 2002. p. 4 (2 pages)
Full text | Page Image - PDF | Abstract

23. **New initiatives bend boards**
Bernard Cole. **Electronic Engineering Times.** Manhasset: Jan 21, 2002. p. 1 (2 pages)
Text+Graphics | Page Image - PDF | Abstract

24. **Optimizing network storage processing performance**
Kim Chan. **Computer Technology Review.** Los Angeles: Jan 2002. Vol. 22, Iss. 1; p. 18 (2 pages)
Text+Graphics | Page Image - PDF | Abstract

25. **ZF announces the first US Coach installation of its AS Tronic automatic transmission**
Anonymous. **Fleet Equipment.** Palatine: Jan 2002. Vol. 28, Iss. 1; p. 44 (1 page)
Full text | Page Image - PDF | Abstract

26. **Functional verification of the POWER4 microprocessor and POWER4 multiprocessor systems**
J M Ludden, W Rosener, G M Heiling, J R Reysa, et al. **IBM Journal of Research and Development.** Armonk: Jan 2002. Vol. 46, Iss. 1; p. 53 (24 pages)
Text+Graphics | Page Image - PDF | Abstract

27. **POWER4 system microarchitecture**
J M Tendler, J S Dodson, J S Field Jr, H Le, B Sinharoy. **IBM Journal of Research and Development.** Armonk: Jan 2002. Vol. 46, Iss. 1; p. 5 (21 pages)
Text+Graphics | Page Image - PDF | Abstract

28. **Finally, a verification GUI**
Donna Mitchell. **ECN.** Radnor: Nov 15, 2001. Vol. 45, Iss. 13; p. 62 (1 page)
Text+Graphics | Page Image - PDF | Abstract

29. **Empowering GPRS handsets with embedded cache**
Afzal Malik, David Gonzales. **Communication Systems Design.** San Francisco: Nov 2001. Vol. 7, Iss.

11; p. 36 (3 pages)

Text+Graphics Page Image - PDF Abstract

30. **The HyperTransport technology I/O bus architecture**
David Rich. **Computer Technology Review.** Los Angeles: Fourth Quarter 2001. p. 8 (6 pages)

Text+Graphics Page Image - PDF Abstract

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Results per page: 10

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1 Performance evaluation of a commercial cache-coherent shared memory multiprocessor 77%

Rajeev Jog , Philip L. Vitale , James R. Callister

ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1990 ACM SIGMETRICS conference on Measurement and modeling of computer systems April 1990

Volume 18 Issue 1

This paper describes an approximate Mean Value Analysis (MVA) model developed to project the performance of a small-scale shared-memory commercial symmetric multiprocessor system. The system, based on Hewlett Packard Precision Architecture processors, supports multiple active user processes and multiple execution threads within the operating system. Using detailed timing for hardware delays, a customized approximate closed queueing model is developed for the multiprocessor system ...

2 Balancing performance and flexibility with hardware support for network architectures 77%

Ilija Hadžić , Jonathan M. Smith

ACM Transactions on Computer Systems (TOCS) November 2003

Volume 21 Issue 4

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

3 Simulation coverage and generation for verification: Coverage-oriented verification of banias 77%

Alon Gluska

Proceedings of the 40th conference on Design automation June 2003

The growing complexity of state-of-art microprocessors dictates the use of cost-effective verification methods. Functional coverage was widely applied in the verification of Banias, Intel's new IA-32 microprocessor designed solely for the mobile computing market. In this paper, we describe the practical coverage approach as was carried out in the verification of Banias. According to this Coverage-Oriented verification approach, focus shifts gradually from basic logic cleanup using random testing ...

4 MEDEA workshop: Fine-grain design space exploration for a cartographic SoC multiprocessor 77%

Alessio Bechini , Pierfrancesco Foglia , Cosimo Antonio Prete
ACM SIGARCH Computer Architecture News March 2003
Volume 31 Issue 1

Traditionally, in the field of embedded systems low power consumption and low cost have been always regarded as stringent specification constraints. In recent years, high computational power has become a fundamental requirement as well. This has been mainly determined by the introduction of new features, typical of general-purpose systems, e.g. GUI-based interfaces. In this setting, low cost, low power consumption, significant computational power and short time-to-market are conflicting needs th ...

5 An architecture for mostly functional languages 77%

Tom Knight
Proceedings of the 1986 ACM conference on LISP and functional programming
August 1986

6 Synchronization with multiprocessor caches 77%

Joonwon Lee , Umakishore Ramachandran
ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture May 1990
Volume 18 Issue 3

Introducing private caches in bus-based shared memory multiprocessors leads to the cache consistency problem since there may be multiple copies of shared data. However, the ability to snoop on the bus coupled with the fast broadcast capability allows the design of special hardware support for synchronization. We present a new lock-based cache scheme which incorporates synchronization into the cache coherency mechanism. With this scheme high-level synchronization primitives as well as low-le ...

7 Compiler techniques for data partitioning of sequentially iterated parallel loops 77%

David E. Hudak , Santosh G. Abraham
ACM SIGARCH Computer Architecture News , Proceedings of the 4th international conference on Supercomputing June 1990
Volume 18 Issue 3

This paper uses bottom-up, static program partitioning to minimize the execution time of parallel programs by reducing interprocessor communication. Program partitioning is applied to a parallel programming construct known as a sequentially iterated parallel loop. This paper develops and evaluates compiler techniques to automatically generate data partitions for sequentially iterated parallel loops that minimize interprocessor communication. These techniques could be included as a communica ...

8 Disk-directed I/O for MIMD multiprocessors 77%

David Kotz

ACM Transactions on Computer Systems (TOCS) February 1997
Volume 15 Issue 1

Many scientific applications that run on today's multiprocessors, such as weather forecasting and seismic analysis, are bottlenecked by their file-I/O needs. Even if the multiprocessor is configured with sufficient I/O hardware, the file system software often fails to provide the available bandwidth to the application. Although libraries and enhanced file system interfaces can make a significant improvement, we believe that fundamental changes are needed in the file server software. We prop ...

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"bus transactions"

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1 **Architectural impact of secure socket layer on Internet servers**
Kant, K.; Iyer, R.; Mohapatra, P.;
Computer Design, 2000. Proceedings. 2000 International Conference on , 17-2
2000
Page(s): 7 -14

[Abstract] [PDF Full-Text (712 KB)] **IEEE CNF**

2 **Bus buffer modeling and optimization in video processing IP**
Kun-Bin Lee; Chia-Hsing Lin; Chein-Wei Jen;
Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEE
International Conference on , Volume: 3 , 5-8 Sept. 1999
Page(s): 1779 -1782 vol.3

[Abstract] [PDF Full-Text (352 KB)] **IEEE CNF**

3 **A bandwidth-efficient implementation of mesh with multiple broadca**
Jong Hyuk Choi; Bong Wan Kim; Kyu Ho Park; Kwang-Il Park;
Parallel Processing, 1999. Proceedings. 1999 International Conference on , 21-
Sept. 1999
Page(s): 434 -443

[Abstract] [PDF Full-Text (244 KB)] **IEEE CNF**

4 **An approach to verify a large scale system-on-a-chip using symbolic checking**
Takayama, K.; Satoh, T.; Nakata, T.; Hirose, F.;

Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceed
International Conference on , 5-7 Oct. 1998
Page(s): 308 -313

[Abstract] [PDF Full-Text (96 KB)] **IEEE CNF**

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5 **Design and performance evaluation of an adaptive cache coherence protocol**
Won-Kee Hong; Nam-Hee Kim; Shin-Dug Kim;
Parallel and Distributed Systems, 1998. Proceedings., 1998 International Confe
on , 14-16 Dec. 1998
Page(s): 33 -40

[Abstract] [PDF Full-Text (152 KB)] **IEEE CNF**

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6 **CPU cache prefetching: Timing evaluation of hardware implementati**
Tse, J.; Smith, A.J.;
Computers, IEEE Transactions on , Volume: 47 Issue: 5 , May 1998
Page(s): 509 -526

[Abstract] [PDF Full-Text (612 KB)] **IEEE JNL**

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7 **Performance analysis using a non-invasive instruction trace mechani**
Sandon, P.A.; Yuchung Liao;
Performance, Computing, and Communications Conference, 1997. IPCCC 1997.
International , 5-7 Feb. 1997
Page(s): 308 -314

[Abstract] [PDF Full-Text (592 KB)] **IEEE CNF**

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8 **Global bus design of a bus-based COMA multiprocessor DICE**
Lee, G.; Quattlebaum, B.; Cho, S.; Kinney, L.;
Computer Design: VLSI in Computers and Processors, 1996. ICCD '96. Proceed
1996 IEEE International Conference on , 7-9 Oct. 1996
Page(s): 231 -240

[Abstract] [PDF Full-Text (964 KB)] **IEEE CNF**

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9 **A shared-bus control mechanism and a cache coherence protocol for high-performance on-chip multiprocessor**
Takahashi, M.; Takano, H.; Kaneko, E.; Suzuki, S.;

High-Performance Computer Architecture, 1996. Proceedings. Second Internati
Symposium on , 3-7 Feb. 1996
Page(s): 314 -322

[Abstract] [PDF Full-Text (704 KB)] **IEEE CNF**

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10 **Boosting the performance of hybrid snooping cache protocols**
Dahlgren, F.;
Computer Architecture, 1995. Proceedings. 22nd Annual International Symposi
on , 22-24 June 1995
Page(s): 60 -69

[Abstract] [PDF Full-Text (1028 KB)] **IEEE CNF**

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11 **A microarchitectural performance evaluation of a 3.2 Gbyte/s microprocessor bus**
Stanley, T.; Upton, M.; Sherhart, P.; Mudge, T.; Brown, R.;
Microarchitecture, 1993. Proceedings of the 26th Annual International Symposi
on , 1-3 Dec. 1993
Page(s): 31 -40

[Abstract] [PDF Full-Text (752 KB)] **IEEE CNF**

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12 **Flexible system interface ASIC for FDDI adapter**
Venkataraman, R.;
Computers and Communications, 1993., Twelfth Annual International Phoenix
Conference on , 23-26 March 1993
Page(s): 127 -133

[Abstract] [PDF Full-Text (540 KB)] **IEEE CNF**

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13 **A bus on a diet-the serial bus alternative-an introduction to the P13 High Performance Serial Bus**
Teener, M.;
Compcon Spring '92. Thirty-Seventh IEEE Computer Society International Conf
Digest of Papers. , 24-28 Feb. 1992
Page(s): 316 -321

[Abstract] [PDF Full-Text (468 KB)] **IEEE CNF**

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14 **VLSI development of a global memory interface controller**

Reiner, T.C.; Lindsey, M.J.;
Military Communications Conference, 1990. MILCOM '90, Conference Record, 'A
Era'. 1990 IEEE , 30 Sept.-3 Oct. 1990
Page(s): 254 -257 vol.1

[Abstract] [PDF Full-Text (308 KB)] **IEEE CNF**

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15 **VLSI support for copyback caching protocols on Futurebus**
Sweazey, P.;
Computer Design: VLSI in Computers and Processors, 1988. ICCD '88., Proceec
the 1988 IEEE International Conference on , 3-5 Oct. 1988
Page(s): 240 -246

[Abstract] [PDF Full-Text (520 KB)] **IEEE CNF**

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